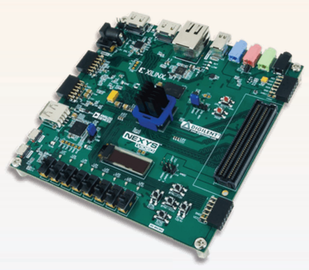
WAVEFORM GENERATION WITH FPGA USING DIGITAL SIGNAL PROCESSING TECHNIQUES

AIM

Signal processing algorithms benefit from parallel computational capabilities, especially where low latency and high throughput are desired. Performance-critical signal processing pipelines are commonly implemented as customized hardware blocks in either application-specific integrated circuit (ASIC) or FPGA chips, due to their phenomenal parallel processing capability and performance determinism. Thus, this project aims to:

- Explore the possibilities of signal generation and digital signal processing (DSP) implemented in a Field-Programmable Logic Array (FPGA) chip.
- Generate fundamental signals and apply various signal processing techniques utilizing an FPGA chip, underscoring the significance and versatility of FPGA chips as a method for generating and processing signals.

MATERIALS & METHODS



Evaluation Board

Nexys Video Artix-7

FPGA evaluation board containing peripherals which aid the research

- Audio Codec
- Xilinx Artix-7 FPGA

Verilog & VHDL

- Hardware Description Language (HDL)
- Synthesis and processing functionalities developed as individual modules
- DDS IP block used for sine wave generation

Modules

Vivado

Integrated software development platform for Xlinx FPGAs

Development Environment

DISCUSSION

This project has demonstrated waveform generation and DSP through FPGA logic, with potential in high-frequency signal generation (such as radio frequencies), and waveform manipulation and modulation.

Limitations

- Verilog code is only limited to the audible range (less than 20kHz) as the signal output port is an audio port on the evaluation board.
- In the reconstruction of the summed sine wave from the Pulse-Width modulated waveform, it should be noted that the reconstruction of the sine wave is less than ideal as the frequency of the PWM is insufficient to capture the higher frequency component of the summed sine wave.

Possible Solutions

- Utilise digital outputs of the FPGA chip directly with a pipeline which produces digital output (e.g., PWM) for higher output frequency.
- Increasing the PWM frequency would allow the summed sine wave to be (more) faithfully recreated.

CONCLUSION

In conclusion, waveforms were generated by the FPGA on the Nexys evaluation board, through an audio port. The characteristics and limitations of the waveforms generated were discussed. Basic digital signal processing techniques were simulated and discussed.

Future Work

- Shift-keying processing pipelines (e.g., Frequency-Shift Keying (FSK))
- Realtime processing pipelines of dynamic input data

RESULTS & ANALYSIS

Signal Synthesis

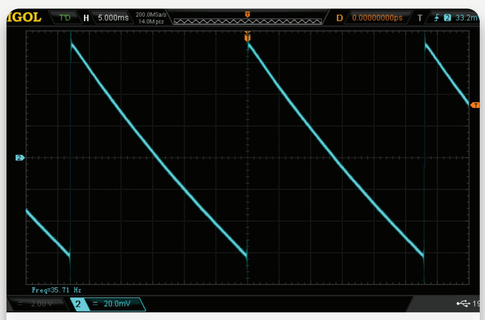


Figure 1: Generated sawtooth waveform

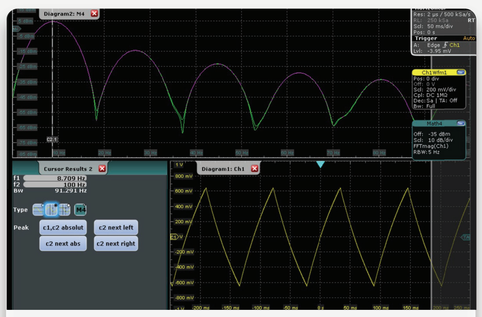


Figure 2: Generated triangle waveform

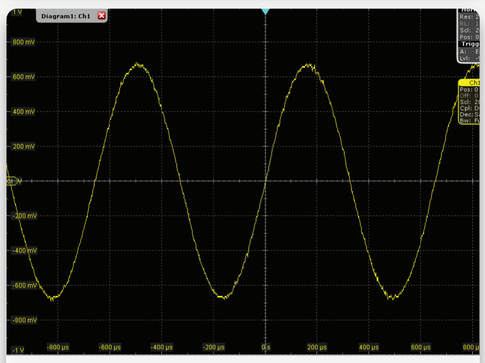


Figure 3: Generated sinusoidal waveform

Figures 1-3 visualize the respective waveforms generated by the FPGA. Figure 4 is a spectrum analysis of the generated sinusoidal waveform

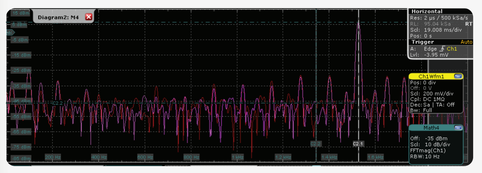
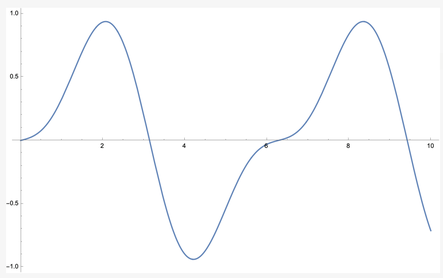


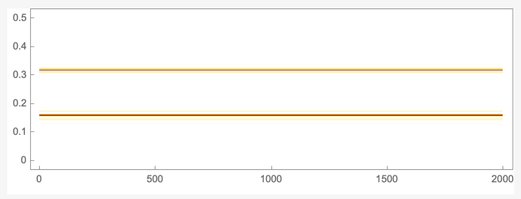
Figure 4: Spectrogram of sinusoidal waveform

Some distortions to the output signal are present due to the inherent non-linearity of the audio codec

Signal Processing

Sine Summation



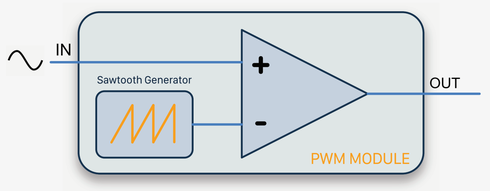


Left: Summation of 2 sine waves
Top: Spectrum analysis of resultant waveform

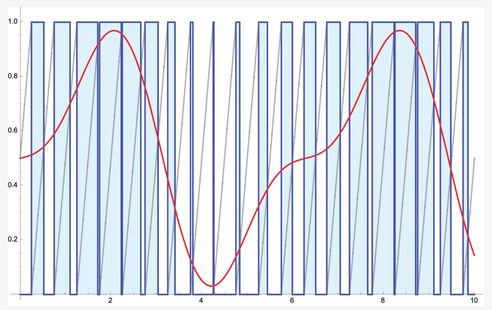
PWM

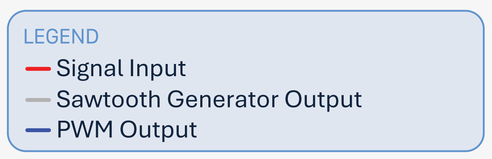
A PWM module which accepts an arbitrary signal and produces a binary output was constructed according to the following block diagram.

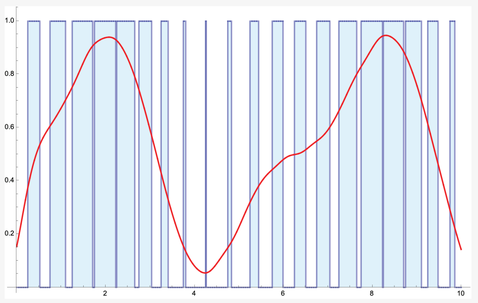
Following this, we can evaluate the performance of the digital PWM signal in reproducing the original analog signal. Do note that the PWM frequency in this case, 2Hz, is relatively low for demonstration purposes especially in comparison to the signal frequency.



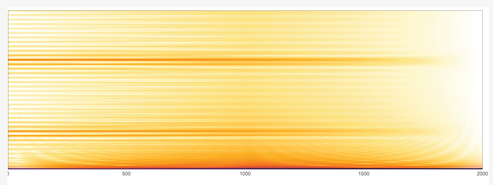
We can see that the reconstructed signal largely resembles the original waveform but has some undesirable distortions, due to the presence of a higher frequency component in the input signal.







Reconstruction of original signal from PWM through low-pass filter



Spectrum analysis of PWM signal: note presence of original signal components

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